Amendments to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the above-identified application.

Listing of Claims:

1. (currently amended) A microinstruction sequencer, comprising:

a microinstruction sequencer stack comprising an array of memory cells; and

microinstruction sequencing logic associated with the microinstruction sequencer stack, wherein the microinstruction sequencing logic determines if a microinstruction affects the microinstruction sequencer stack by determining if the microinstruction includes an operations encoding defined to control the microinstruction sequencer stack.~~to determine if there are any microinstructions being issued which affect the microinstruction sequencer stack.~~

2-3. (cancelled)

4. (original) The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to:

generate a value of a microinstruction address;

add an intermediary value to the value of the microinstruction address to yield an incremented value;

send a control value to the microinstruction sequencer stack, said control value to cause the incremented value to be pushed onto the microinstruction sequencer stack; and

push the incremented value onto the microinstruction sequencer stack.

5. (original) The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to:

send a control value to the microinstruction sequencer stack, said control value to:

cause the microinstruction sequencer stack to pop a value; and

send the popped value to a microinstruction address multiplexer.

6. (currently amended) The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to:

send a control value to the microinstruction sequencer stack, said control value to:

cause the microinstruction sequencer stack to pop a value; and

send the popped value to an immediate logic, said immediate logic to pass the value to ~~the~~ a microprocessor core unit.

7. (original) The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack, said control value to cause the microinstruction sequencer stack to push a value in an immediate field of a microinstruction onto the microinstruction sequencer stack.

8. (original) The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack, said control value to cause the microinstruction sequencer stack to return to a reset state.

9. (original) The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack, said control value to cause the microinstruction sequencer stack to pop a value and send the popped value to an immediate logic.

10. (original) The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack, said control value to cause the microinstruction sequencer stack to send a value at the top of the microinstruction sequencer stack to an immediate logic.

11-12. (cancelled)

13. (currently amended) A microprocessor including a microinstruction sequencer comprising:

an array of memory cells dedicated to ~~said~~ a microinstruction sequencer stack;

an address multiplexer coupled to ~~said~~ the array of memory cells;

sequencing logic coupled to ~~said~~ the address multiplexer and to ~~said~~ the array of memory cells, wherein the sequencing logic determines if a microinstruction affects the microinstruction sequencer stack by determining if the microinstruction includes an operations encoding defined to control the ~~includes logic to determine if there are any microinstructions being issued which affect the~~ microinstruction sequencer stack; and

a microprocessor core unit coupled to ~~said~~ the array of memory cells.

14. (original) The microinstruction sequencer of claim 13, wherein the microprocessor core unit is an execution unit.

15. (original) The microinstruction sequencer of claim 13, wherein the microprocessor core unit is a retire unit.

16-17. (cancelled)

18. (new) A microinstruction sequencer, comprising:

a microinstruction sequencer stack comprising an array of memory cells; and

microinstruction sequencing logic associated with the microinstruction sequencer stack, wherein the microinstruction sequencing logic determines if a microinstruction affects the microinstruction sequencer stack by determining if operation code is present in a field in the microinstruction reserved for microinstruction sequencer stack operations.

19. (new) A microprocessor including a microinstruction sequencer comprising:

an array of memory cells dedicated to a microinstruction sequencer stack;

an address multiplexer coupled to said array of memory cells;

sequencing logic coupled to the address multiplexer and to the array of memory cells,

wherein the sequencing logic determines if a microinstruction affects the microinstruction sequencer stack by determining if operation code is present in a field in the microinstruction reserved for microinstruction sequencer stack operations; and

a microprocessor core unit coupled to the array of memory cells.

20. (new) The microinstruction sequencer of claim 18, wherein the microinstruction sequencing logic includes logic to:

generate a value of a microinstruction address;

add an intermediary value to the value of the microinstruction address to yield an incremented value;

send a control value to the microinstruction sequencer stack, said control value to cause the incremented value to be pushed onto the microinstruction sequencer stack; and

push the incremented value onto the microinstruction sequencer stack.

21. (new) The microinstruction sequencer of claim 18, wherein the microinstruction sequencing logic includes logic to:

send a control value to the microinstruction sequencer stack, said control value to:

cause the microinstruction sequencer stack to pop a value; and

send the popped value to a microinstruction address multiplexer.

22. (new) The microinstruction sequencer of claim 18, wherein the microinstruction sequencing logic includes logic to:

send a control value to the microinstruction sequencer stack, said control value to:

cause the microinstruction sequencer stack to pop a value; and

send the popped value to an immediate logic, said immediate logic to pass the value to a microprocessor core unit.

23. (new) The microinstruction sequencer of claim 18, wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack, said control value to cause the microinstruction sequencer stack to push a value in an immediate field of a microinstruction onto the microinstruction sequencer stack.

24. (new) The microinstruction sequencer of claim 18, wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack, said control value to cause the microinstruction sequencer stack to return to a reset state.

25. (new) The microinstruction sequencer of claim 18, wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack, said control value to cause the microinstruction sequencer stack to pop a value and send the popped value to an immediate logic.

26. (new) The microinstruction sequencer of claim 18, wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack, said control value to cause the microinstruction sequencer stack to send a value at the top of the microinstruction sequencer stack to an immediate logic.

27. (new) The microinstruction sequencer of claim 19, wherein the microprocessor core unit is an execution unit.

28. (new) The microinstruction sequencer of claim 19, wherein the microprocessor core unit is a retire unit.